

Keysight Technologies

Overcoming Limited Access with Cover-Extend Technology at In-Circuit Test

Case Study

Background

The computer industry is facing technical challenges in their motherboard manufacturing test due to the introduction of a new generation of central processing unit (CPU) sockets and ball grid array (BGA) devices with higher pin counts. This case study illustrates how the Keysight Technologies, Inc. Cover-Extend technology, which is part of the *Medalist* VTEP v2.0 Powered vectorless test suite, can help to enable test access for situations where test access becomes increasingly limited with usage of high complexity components on computer motherboards.

This article was first published in *Circuits Assembly*, January 2009, and is republished here with kind permission from UP Media Group.

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Manufacturing test challenges

The higher pin counts on CPU sockets and BGA devices along with high speed differential signals are posing new challenges to existing In-Circuit Test of motherboard printed circuit board assemblies (PCBA) on the manufacturing floor.

The following are the manufacturing test challenges:

1. The new generation CPU sockets consist of about 55% signal pins. Most of these signal pins are high speed differential signals that are no longer accessible for ICT probing (see Figure 1).
2. The demand for smaller, low cost computers is also driving down the size of the motherboard, causing constraint in the PCB size and loss of access for ICT.
3. Too many ICT probes under the BGA devices or CPU socket can result in solder ball crack (Figure 2).
4. How to lower the cost of test without sacrificing test coverage.



Figure 1. Hidden trace without access between BGA device ball and CPU socket ball

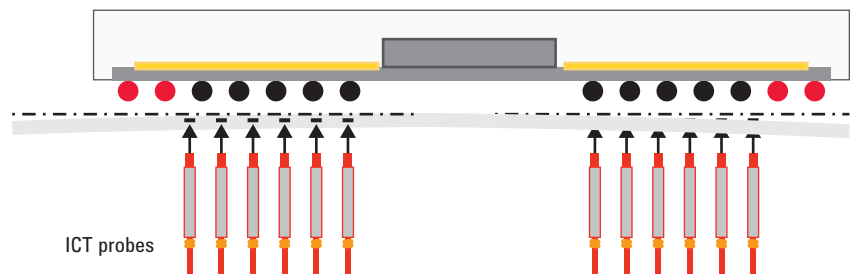


Figure 2. Too many ICT probes under a BGA device will cause the board to flex and strain the solder balls

The solution

Keysight's Cover-Extend Technology is a hybrid between VTEP and Boundary Scan. It draws the best from what each technology offers and enhances the overall capability of Keysight in-circuit test systems. In short, VTEP and Boundary Scan are the main building blocks providing coverage extension for manufacturers even as fewer test points are accessible these days.

VTEP (Vectorless Test Extended Performance)

The Keysight VTEP unpowered vectorless test method uses a stimulus signal that is driven by the in-circuit probe using a sensor plate to measure the capacitance between device pins or BGA balls and the printed circuit board (PCB) pads. Figure 3 shows the number of pins tested on a circuit using VTEP test.

The VTEP methodology requires physical test access (i.e. test probes) to deliver this stimulus signal. With Cover-Extend, however, the stimulus signal is delivered via a Boundary Scan device.

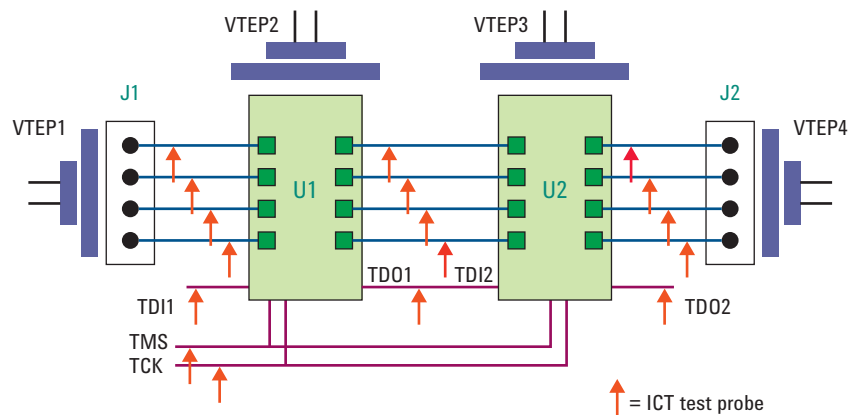


Figure 3. ICT using VTEP

The solution

Boundary Scan

Boundary Scan is a world-wide standardized test methodology (IEEE 1149.x standard). It provides limited-access capability – i.e., the ability to control the I/O functions of individual pins through the use of only four pins on the test access port. Figure 4 shows the number of pins tested on a circuit using Boundary Scan test.

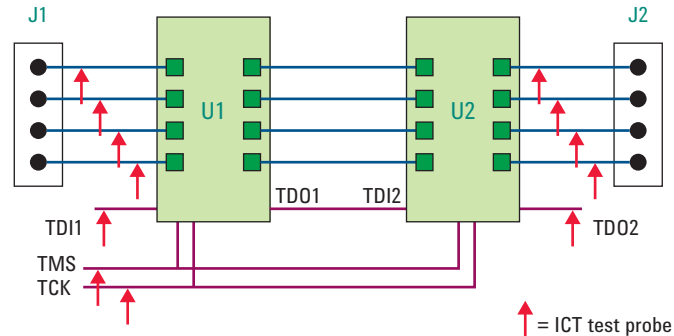


Figure 4. ICT test using Boundary Scan

The Keysight Cover-Extend Technology

Cover-Extend works as follows:

1. The VTEP sensor, which is able to capacitively pick up stimulus signals, is placed on the component to be tested (e.g. a connector).
2. The Boundary Scan device does not require test probes on every pin.
3. As per the IEEE 1149.x standard, using only the test access port, users can deliver the necessary stimulus signal to the connector.
4. A defect (e.g. an open) on the path between the Boundary Scan device and the VTEP sensor will affect the stimulus signal that is bound for the sensor.
5. The result is captured and diagnosed by the ICT system and thus, the defect is detected.

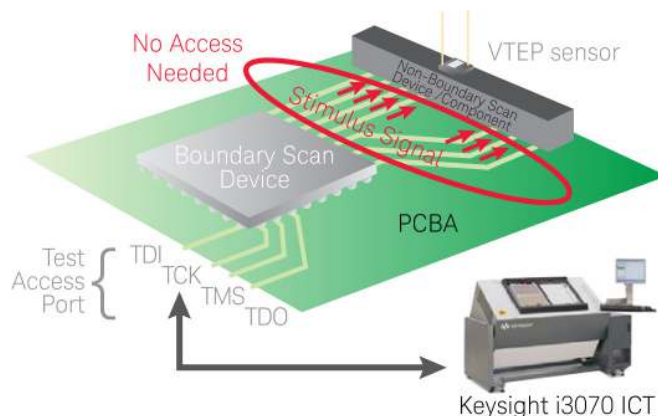


Figure 5. Keysight Cover-Extend technology

The solution

Cover-Extend minimizes the number of probes required to test the PCBA (See Figure 6 and Table 1) with the same test coverage, using a combination of VTEP and Boundary Scan test.

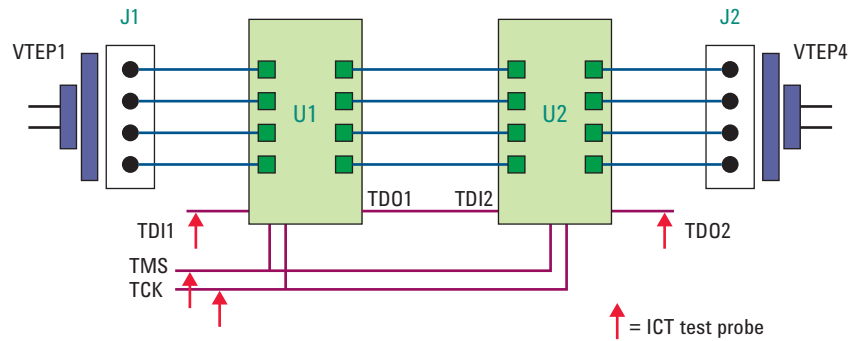


Figure 6. ICT test using Cover-Extend

Table 1. Data study indicates that Cover-Extend is able to provide better coverage while simultaneously requiring fewer test probes

Test strategy	Total number of nodes	Total number of probes	Device coverage
VTEP only	19	17	U1, U2, J1 and J2 tested using VTEP (refer to Figure 3)
Boundary Scan only	19	12	U1, U2 tested using Boundary Scan chain and connect test (refer to Figure 4)
Cover-Extend	19	4	U1, U2, J1 and J2 tested using Boundary Scan chain and Cover-Extend (refer to Figure 6)

The application

Cover-Extend on motherboard

The new generation of motherboards consists mainly of CPU sockets, Input/Output (I/O), BGA devices and power circuitry where in about 50% of the total targeted testable pins and solder balls are CPU sockets and connectors. Traditionally, CPU sockets and connectors are tested at ICT using vectorless testing. However, these test strategies are rapidly eroding as the designers are not able to place test points at every signal pin and solder ball on the motherboard, forcing the test engineers to look for an alternative test strategy.

Results from a study using Cover-Extend on a Keysight *Medalist* i3070 In-Circuit Test system are shown in Figure 7. The data shows the difference between good signal pins and open pins.

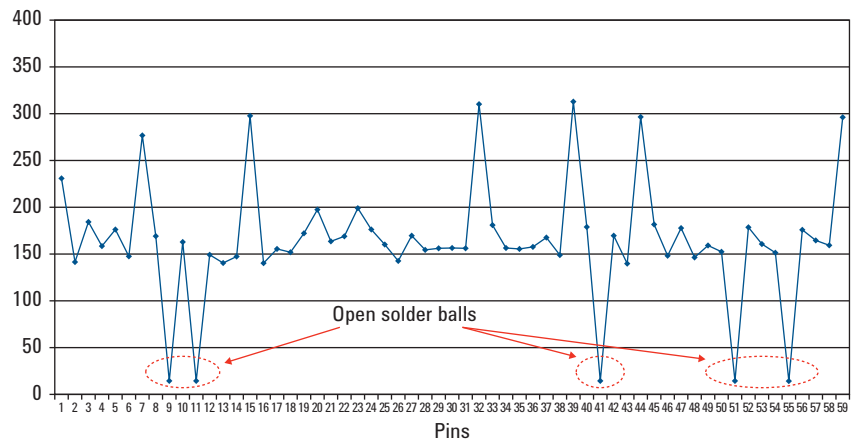


Figure 7. Cover-Extend measurement results for CPU socket with open solder balls

The application

Notebook motherboard

New generation notebook motherboards are seeing dramatic changes in their design, driven by cost pressure, size reduction, as well as demands for longer battery life and increased performance. Notebook motherboard PCBs will continue to shrink in size even as they need to be able to accommodate the new generation of CPU and BGA devices and meet the various demands mentioned above.

Figure 8 shows the number of pins tested using Cover-Extend, with pin coverage of 45% (370 of the total 818 signal pins) on the connectors. In reality, Cover-Extend pin-count coverage includes not only the connector pins, but also the pins of upstream Boundary Scan devices used to drive the signal for Cover-Extend test. Table 2 also shows the number of ICT probes removed when Cover-Extend is used as a test strategy compared to VTEP only, which requires ICT probes to every target pin to be tested.

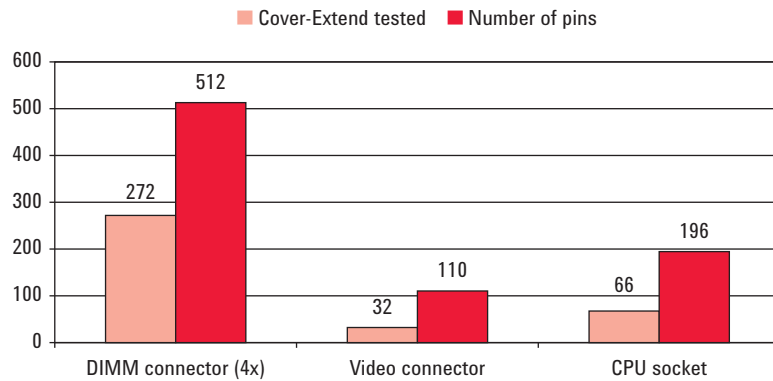


Figure 8. Number of pins tested using Cover-Extend on notebook motherboard

Table 2. Data from actual notebook case study indicates that Cover-Extend is able to provide better coverage while simultaneously requiring fewer test probes

Test strategy	Total number of pins	Total number of probes removed	Device coverage
If using VTEP only	818	0	DDR DIMM, video connector, CPU socket and an I/O chipset tested using VTEP only
If using Boundary Scan only	Not applicable	Not applicable	The Boundary Scan device I/O chipset is not designed in a chain with another Boundary Scan device
Cover-Extend	370	370	DDR DIMM, video connector, CPU socket and an I/O chipset tested using Boundary Scan chain and Cover-Extend

The application

Server motherboard

Server motherboards present the most potential for Cover-Extend usage due to the huge number of connector pins in the server motherboard (See Figure 9).

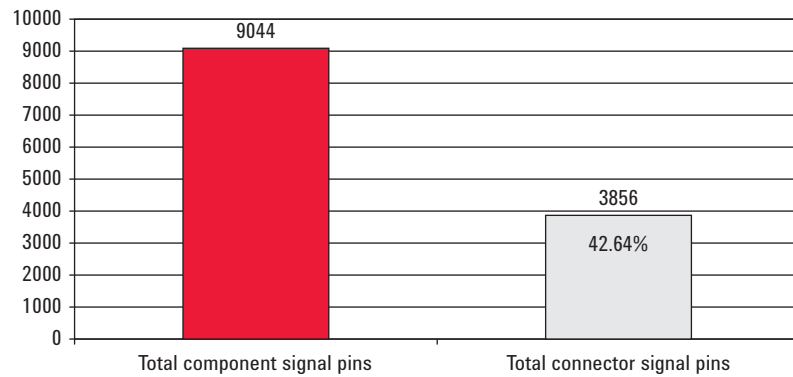


Figure 9. This chart shows the total number of component signal pins versus total connector signal pins on a typical server motherboard

Note: Total component signal pins includes all the components in the motherboard (capacitor, resistor, inductor, diode, transistor, integrated circuit, BGA devices and connectors)

The current server motherboard design still does not have the full capability to maximize Cover-Extend usage as most of the BGA devices are not enabled for Boundary Scan. If the connectors on the server motherboard are to be 100% tested using Cover-Extend, the coverage will also extend to the upstream Boundary Scan devices (see Figure 10).

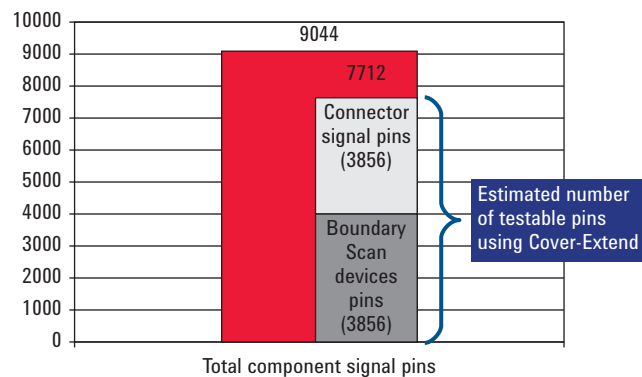


Figure 10. Estimated number of testable pins using Cover-Extend

The application

Another key benefit of using Cover-Extend is the obvious further reduction in the number of ICT probes needed to test all the board components (see Figure 11). The ICT system cost will be reduced as the number of hybrid cards required to test a server motherboard with over 4,000 nodes will also be reduced (see Figure 12).

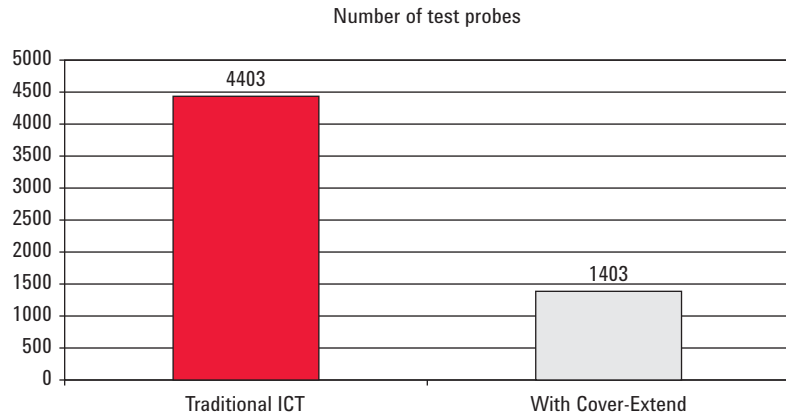


Figure 11. Estimated potential ICT probe requirements using Cover-Extend on a server motherboard with over 4,000 nodes

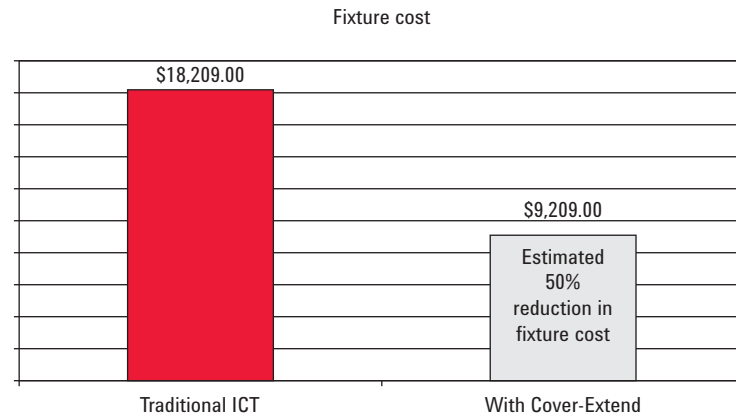


Figure 12. Estimated potential ICT fixture cost using Cover-Extend on a server motherboard with over 4,000 nodes

Note: Assumption of one (1) ICT probes is equivalent to US \$5 (test probes + receptacle + personality pins + drilling cost + wiring and labor cost)

Cover-Extend will also reduce potential solder ball crack occurrences under the BGA and CPU socket as the number of ICT test probes needed will be reduced almost by half, minimizing the strain on the PCB.

References

1. Keysight Medalist VTEP v2.0 Powered with Cover-Extend Technology 5989-8429EN
2. Maximizing Test Coverage with Keysight Medalist VTEP v2.0 – VTEP, iVTEP and NPM 5989-6344EN

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